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L31	l20 and L30 and l26 and l22 and l4	4	L31
L30	polarity same l1	199	L30
L29	l27 and L28	12	L29
L28	polarity same voltage	61405	L28
L27	l20 and L26 and l22 and l4 and l1	18	L27
L26	latch$3	194286	L26
L25	l19 and L24	0	L25
L24	voltage and L23	30	L24
L23	l20 and L22 and l15 and l11 and l6 and l1	34	L23
L22	((379/$)!.CCLS.)	42659	L22
L21	l16 and L20	11	L21
L20	reversal	73990	L20
L19	l16 and L18	12	L19
L18	surge	37213	L18
L17	l1 and L16	2	L17
L16	l14 and L15	43	L16
L15	period$5	1012378	L15
L14	l4 and l13	48	L14
L13	voltage and l12	97	L13
L12	l10 and L11	99	L12
L11	polarity	148753	L11
L10	l8 and l6	248	L10
L9	l7 and L8	1	L9
L8	optocoupler	1502	L8
L7	l5 and L6	58	L7
L6	flip flop or flipflop	79197	L6
L5	l3 and L4	242	L5
L4	discharge and charge	116616	L4
L3	l1 and L2	1430	L3
L2	tip and ring	82622	L2
L1	onhook or on-hook	4632	L1

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DATE: Sunday, June 15, 2003 Printable Copy Create Case

L36: Entry 5 of 35 File: USPT Feb 4, 1992

DOCUMENT-IDENTIFIER: US 5086459 A
TITLE: Timing circuit and a secure telephone jack utilizing this circuit

Abstract Text (1):
A timing circuit and apparatus that utilizes this circuit. The apparatus is particularly suited for use with a telephone network interface, for substantially preventing a third party who gains access to the interface from placing an unauthorized telephone call through a network connection obtained through a jack, typically modular, located in a customer portion of the interface. Specifically, this apparatus is connected in series within the telephone company side of the interface to illustratively a ring lead of an incoming subscriber loop. In operation, the apparatus provides network access, by supplying loop current, on a timed periodic (repetitive) basis to a telephone (or other equipment through which a telephone call can be placed) plugged into the jack located within the network interface. Access is provided for a period of time that is sufficient to test loop current but is insufficient to allow the network to complete a call dialed from that telephone over this loop. However, between any two successive intervals during which the apparatus supplies loop current to the telephone, the apparatus interrupts this current for a period of time that is sufficient for a switching machine at a local central office that serves this loop to interpret the cessation of current as an on-hook condition, completely terminate any call that may be in progress for this telephone and reset the loop.

Brief Summary Text (13):
Specifically, in accordance with the teachings of my present invention, my inventive apparatus is connected in series within the telephone company side of the interface to illustratively a ring (or tip) lead of an incoming subscriber loop. In operation, my apparatus provides network access, by supplying loop current, on a timed periodic (repetitive) basis to a telephone (or other communication equipment through which a telephone call can be placed) plugged into a telephone jack, typically a modular jack, located within the network interface. Access is provided for a period of time that is sufficient to test dial tone but is insufficient to allow the network to complete a call dialed from that telephone over this loop. However, between any two successive intervals during which the apparatus supplies loop current to the telephone, this apparatus interrupts this current for a period of time that is sufficient for a switching machine at a local central office that serves this loop to interpret the cessation of current as an on-hook condition, completely terminate any call that may be in progress for this telephone and reset the loop.

Detailed Description Text (9):
Specifically, telephones are conventionally and generally universally wired such that subscriber loop connections appear on pins three and four (similarly marked in FIG. 1) of a modular plug connected thereto, here plug 50. In telephone network interfaces known in the art, network connections are brought directly to pins three and four of the modular jack. Hence, if telephone 80 were to be plugged into a modular jack situated within a well-known telephone network interface, then that telephone would have unrestricted access to the network, thereby permitting a third party caller to place unauthorized calls through the network via subscriber loop 11. In accordance with my invention, these unrestricted network access connections are moved to non-standard pins, specifically pins two and five, on modular jack 40. Modular plug 50 is similarly wired such that the unrestricted network access connections are extended via leads 63 and 69 to terminals 73 and 77 for connection to the customer premise wiring. Pins three and four of jack 40 are wired to provide access restricted rather than unrestricted connections. Specifically, tip lead 23 associated with subscriber loop 11 is extended, via leads 23 and 25, which are

connected together, to pins two and three of jack 40 and therethrough to mating pins two and three of plug 50. Next, ring lead 27 associated with subscriber loop 11 is wired to an input of timed network access circuit 30. From there, lead 37 routes the output provided by circuit 30 to pin four of jack 40. Once loop voltage is applied by a central office to subscriber loop 11, circuit 30, as noted above, interrupts loop current on ring lead 37 and hence on two wire loop 64 on an oscillating (repetitive) illustrative eight second on, two second off pattern. The eight-second on time of the loop current is simply insufficient for the telephone network to complete a call dialed from telephone 80. During the two-second off time, a switching machine at a local central office that serves subscriber loop 11 will simply interpret the cessation of loop current as an on-hook condition, completely terminate any call then in progress for this telephone and reset the loop. As such, telephone 80, by virtue of its universal interconnect wiring and when plugged into modular jack 40, will only receive, via loop 64, restricted network access as provided by circuit 30. Ring lead 27 is also routed via lead 29 to pin five of jack 40. However, through mating pins two and five of jack 40 and plug 50, a customer will receive unrestricted network access through leads 23 and 29 associated with loop 11 and leads 63 and 69 associated with loop 61. Although circuit 30 is shown as being situated on the ring lead for telephone 80, this circuit could just as easily be situated on the tip lead therefor inasmuch as loop current to this telephone can be interrupted through either lead. Likewise, pins 1 and 6 may be substituted for pins 2 and 5, as any other non-standard wiring connection may be chosen.

Detailed Description Text (13):
Bridge rectifier 200 couples switch 210, which is typically uni-polar, to a potentially unknown direction of loop current, i.e. that which flows through the ring side of the subscriber loop. This, in turn, greatly simplifies the installation of circuit 30 to the subscriber loop. Inasmuch as the ring lead can easily become reversed in a field installation, bridge rectifier 200 enables circuit 30 to be polarity insensitive to the direction of loop current flowing through leads 27 and 37 and thereby properly function under a line reversal condition. Moreover, since switch 210 can be uni-polar rather than multi-polar, a wide variety of different voltage or current controlled solid state devices can be used to implement switch 210. For example, these devices could encompass a bipolar transistor or even a well known Darlington configuration, provided the values of capacitance and resistance used within circuit 30 are kept within practical limits consistent with any additional voltage drop that appears across these devices, when conducting, as compared to that appearing across a conducting FET. Clearly, a FET or similar device is preferable to a bipolar transistor(s) inasmuch as both the resistance and associated voltage drop appearing across a conducting FET may be lower and the gate resistance is substantially higher than the on resistance, voltage drop and base resistance, respectively, that are associated with a bipolar transistor. It should be noted here that switch 210 should not be implemented using a thyristor inasmuch as loop current can be interrupted or even reverse its direction (both of which entail that the current becomes or passes through a zero value) during a wide variety of normal loop and network conditions, such as during a request for service or dial tone, that occur in some telephone systems. Once this loop current decreases below a minimal value required to maintain the thyristor in conduction, the thyristor would become blocking. As such, the thyristor would then need to be triggered on to accommodate the loop current that flows immediately after any such interruption or reversal which, in turn, would disadvantageously complicate the gating circuitry of the thyristor and increase the expense of circuit 30.

Detailed Description Text (15):
To readily understand the operation of circuit 30, as shown in FIG. 3, assume that FET 320 has just been de-energized. As such, loop current is interrupted with voltage appearing across output leads 203 and 207 of bridge rectifier 200. This causes the voltage appearing across capacitor 346 to increase at a rate determined by the time constant defined by the values of resistor 342 and capacitor 346. Now assuming that the voltage appearing across capacitor 334 is initially zero, then once the voltage appearing across capacitor 346 and hence across diode 336 reaches the breakover potential of this diode, which is illustratively and approximately 18 volts, this diode enters its negative resistance region and begins to conduct. Since, at this point, capacitor 334 is discharged, charge is very quickly transferred from capacitor 346 to capacitor 334 to equalize potentials appearing

across both of these capacitors. As a result, current flow between these two capacitors rapidly decreases to zero thereby, as discussed below, turning off diode 336. Consequently, the voltage appearing across capacitor 334 rapidly increases and, being applied to the gate of FET 320, reaches a level sufficient to energize the FET. Once the FET is energized, it provides a low resistance path between leads 203 and 207 thereby permitting loop current to flow through bridge rectifier 200 and between leads 27 and 37. At the same time, this low impedance path provides a discharge path through resistor 342 and diode 344, if the latter is used, to rapidly discharge capacitor 346 while FET 320 is conducting. Once the voltages appearing across discharging capacitor 346 and capacitor 334 become equal, diode 336 enters its high impedance state due to insufficient holding current and ceases to conduct, thereby isolating circuit 230 from circuit 220. Furthermore, once this diode ceases to conduct, capacitor 334 starts discharging through resistor 332. Inasmuch as the gate of FET 320 presents a substantial input impedance, the rate at which the voltage across capacitor 334 and the gate voltage to the FET decays is determined by the time constant defined by the values of resistor 332 and capacitor 334. This time constant is set such that the voltage appearing across this capacitor will remain above the turn-on voltage for FET 320 for approximately eight seconds. Accordingly, FET 320 will remain on and conduct loop current for this time. Once the voltage appearing across capacitor 334 discharges below the turn-on gate voltage of FET 320, the FET de-energizes to interrupt loop current. Voltage then appears across leads 203 and 207 to initiate the charge cycle for capacitor 346. While capacitor 346 is charging and before the voltage appearing across diode 336 reaches its breakover potential, capacitor 334 continues to discharge through resistor 332 to approximately zero. The time constant associated with capacitor 334 is significantly longer than the time constant associated with capacitor 346. This time constant associated with capacitor 346 is set such that the FET 320 remains de-energized for approximately two seconds. Now, when the voltage appearing across diode 336 again reaches its breakover potential, the operation of circuit 30, as described above, simply repeats and so on to provide alternating periods of switched loop current: eight seconds on followed by two seconds off. The breakdown voltage of diode 336 and the values of capacitors 334 and 346 are all chosen such that the peak voltage that appears across these capacitors does not exceed the breakdown potential of FET 320 or of the capacitors themselves.

Detailed Description Text (17):
With the component values set forth above and loop current routed through circuit 30, this circuit is designed to operate with standard 48 volt telephone systems and interrupt loop current approximately every eight seconds for an approximately two second period. If operation is desired with other telephone voltages, then the component values, specifically the breakover value and possibly the type of device used for diode 336 may need to be changed accordingly. To provide a version of my inventive circuit that provides similar performance yet operates with a variety of different loop voltages, resistor 342 could be replaced with a constant current source, such as that implemented for example in a well known manner using a junction FET and a few additional parts. Doing so would provide similar charging times for capacitor 346 and similar two second off-times for circuit 30 with variations in loop voltage.

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L7: Entry 11 of 39 File: USPT Aug 4, 1981

DOCUMENT-IDENTIFIER: US 4282407 A
**** See image for Certificate of Correction ****
TITLE: Telephone loop resistance detector

Brief Summary Text (6):
In order to provide automatic adjustment to the length of the connected subscriber loop, it is customary to detect the level of current flow in the loop since such current flow is an indirect measure of the resistance, and hence the length, of the subscriber loop. In the presence of changing central office voltages or voltage reversals at the central office, such current detectors may become inoperative or may indicate an erroneous length of the loop. Providing separate current detectors for each polarity of central office voltage is expensive and does not guarantee accurate detection of subscriber loop length.

Brief Summary Text (9):
In accordance with the present invention, both the loop current in the subscriber loop and the voltage across the subscriber loop are detected. Signals representing these values are used to detect the resistance of the connected subscriber loop independent of the magnitude or polarity of the voltage applied to that loop. In this way, the detection circuits are made independent of the central office voltage and, indeed, provide consistent indications even in the presence of rapid changes in that voltage.

Detailed Description Text (18):
In FIG. 5 there is shown a detailed circuit diagram of the central office voltage detector 12 of FIG. 1 which is connected between tip conductor 10 and ring conductor 11. Tip conductor 10 is connected through resistor 170 to the negative input of differential amplifier 171, while ring conductor 11 is connected to a voltage divider comprising resistors 172 and 173. The junction of resistors 172 and 173 is connected to the positive input of amplifier 171. Feedback resistor 174 is connected from the output of amplifier 171 to the negative input. As previously discussed in connection with FIG. 3, amplifier 171 provides an output signal linearly related to the voltage between conductors 10 and 11, both in magnitude and in polarity.

Detailed Description Text (19):
The output of amplifier 171 is connected through resistors 175 and 176 to positive voltage source 177. The output of amplifier 171 is also connected through resistor 178 and inverter circuit 179 to one input of NAND gate 180. The junction of resistors 175 and 176 is connected to the other input of gate 180. Resistors 175 and 176 and gate 180 establish a voltage threshold referenced to leads 10 and 11 of about 10 volts. Similarly, resistor 178 and inverter 179 establish a voltage threshold of about 10 volts for the other polarity of central office voltage appearing across conductors 10 and 11. The output of NAND gate 180 is therefore a binary or two-state output on lead 181 which indicates that the .+-.10-volt threshold level between conductors 10 and 11 has been exceeded. This threshold is set to detect the loss of the normal central office battery voltage which occurs just prior to the operation of the central office switching crosspoints. In applications such as that shown in FIG. 9, all voltages are removed from the tip and ring conductors prior to each switching operation so that the switching elements do not have to interrupt or initiate current flows as they are operated (i.e., they are operated "dry"). The output of the detector in FIG. 5 on lead 181 is therefore used to rapidly release both L relay 16 and RO relay 17, thereby

removing the range extension circuitry from the circuit during central office switching. The manner in which this is accomplished will be discussed in more detail in connection with FIG. 7.

Detailed Description Text (20):
In FIG. 6 there is shown a detailed circuit diagram of a three-level loop resistance detector. The resistance detector of FIG. 6 responds to the loop current sensor 34, shown in FIG. 1, the output of which appears on conductor 116 in FIG. 6, and the output of the loop voltage sensor of FIG. 3, the output of which appears on lead 125 in FIG. 6. The detector of FIG. 6 comprises three differential amplifiers 200, 201 and 202. Each of these amplifiers is arranged to detect a different resistance level for either polarity of central office battery voltage. Amplifier 200, for example, is designed to detect loop resistances which are less than 1700 ohms (the low resistance threshold). Amplifier 201 is arranged to detect loop resistances that exceed a high threshold of 4300 ohms and amplifier 202 is arranged to detect resistances exceeding a medium threshold of 2200 ohms.

Detailed Description Text (26):
A gate-by-gate explanation of the logic circuit operation is given later; a brief abstract is presented here to illustrate the overall operation. Since the polarities of the loop voltage and loop current are important to successful operation and since, for a given threshold, i.e., TH, only one amplifier (such as amplifier 201) is used to provide the threshold for dual-polarity detection, logic circuits connecting to the amplifier process the amplifier output along with inputs which come from the loop voltage detector amplifier 120. The logic circuit output to resistors 305 and 317 is low for either polarity of voltage which is greater than about 10 volts as seen at the loop voltage detector when the loop resistance is less than the threshold level of the amplifier 201. The following table summarizes the loop voltage detector and loop current detector inputs to the TH amplifier and the logic circuit and shows the output logic level for each set of inputs.

Detailed Description Text (27):
A dial pulse detection circuit is connected across resistor 221. A capacitor 235 is connected in parallel with resistor 221 by the contact 236 of RO relay 17 (FIG. 1). In operation, RO relay 17, and hence RO contact 236, operates in response to an off-hook signal received from the subscriber end of the loop. Dial pulses are represented by transitions between loop resistances of a low value (closed circuit) and loop resistances of a high value (open circuit). However, since the capacitance of the telephone loop must be charged or discharged on each dial pulse transition, the apparent loop resistance rises rather slowly when the dial contacts open and the line capacitance is charged. An oscillatory effective resistance is produced when the dial contacts open the loop and the line also charges the ringer circuit. In order to accurately track dial pulses, it is therefore desirable to provide a high resistance threshold when the dial contacts close the loop and a much lower threshold when the dial contacts open the subscriber loop. This variable threshold provides more accurate detection of the transition times and avoids false indications (split pulses) due to oscillatory peaks in the line resistance by providing a controlled rate of transition from one threshold to the other which masks the ringer charging current oscillations. Capacitor 235 is charged prior to the dial contact opening and thus provides the lower resistance threshold for amplifier 201. When the dial contact closes, capacitor 235 charges through resistor 222 to provide the higher resistance threshold for amplifier 201. Thus, when the dial pulse terminates, a new and higher threshold is provided to amplifier 201 and the dial pulse's termination is detected at a different threshold than the dial pulse initiation. Moreover, the shift is threshold is proportional to the loop current, thus tending to track the dial pulse amplitude.

Detailed Description Text (28):
Amplifier 201 is also used to provide an indication of ring trip. That is, amplifier 201 must detect the current flow due to the operation of the subscriber's switchhook when he goes off-hook in response to ringing signals. This requires a relatively small direct current to be detected in the presence of the alternating

high voltage and high current 20 Hz ringing signals. When ringing occurs, as indicated by ringing detector 14 (FIG. 1), the inhibit signal on lead 160 (FIG. 6) is removed from across resistor 239 and the control electrodes of FETs 240 and 251. FETZ 240 therefore operates to connect a capacitor 241 from positive input 223 of amplifier 201 to ground potential. Capacitor 241 filters out the large varying alternating current component on the subscriber loop caused by the ringing signals but slowly builds up a net charge due to the direct current signal, thereby permitting amplifier 201 and logic circuits (FIG. 7) to detect the small direct current off-hook signal with considerably greater sensitivity. A resistor 242 is connected across capacitor 241 to discharge capacitor 241 when it is not in use. FET 251 connects resistor 250 from input 220 of amplifier 201 to ground. This shifts the detection threshold to account for the lower superimposed direct current (38 volts versus 48 volts).

Detailed Description Text (29):
The ring-trip detection threshold is further defined by the design of the dynamic range of the loop voltage detector so that during ringing the output of the loop voltage amplifier 120 clips the peak of the larger (absolute magnitude) 20 Hz voltage crest. The clipping at the extremities of the loop voltage amplifier 120 output therefore provides a reference voltage for a portion of each 20 Hz cycle to measure the voltage output of the loop current detector against. Ring-trip detection, as a result, is a current threshold measurement rather than a resistance threshold measurement. The TH amplifier 201 and the logic circuits supply drive to resistors 305 and 317 when the dc component of the ringing circuitry exceeds the threshold of the amplifier 201 for a fraction of each 20 Hz cycle. Filtering in the RO relay logic circuit delays the RO relay operation. The L relay operation is fast enough to follow the LOW logic level inputs to its driver. The L relay operates during each high level voltage peak of the ringing voltage waveform. It follows then that the period L contact closures selectively aid the closure of the loop by causing rectified high current pulses to flow through diode 38 (FIG. 1) that reenforce the loop ring-trip signal. The logic circuits act, as detailed in the table, to track the instantaneous polarity of loop voltages during the ringing intervals to make ring-trip detection possible for either polarity of ring-trip battery when applied to either tip or ring conductors.

Detailed Description Text (34):
The output of NAND gate 303 is also applied through a delay circuit comprising diode 342, resistor 343 and capacitor 346 to inverter 341. The input to inverter 341 is normally biased from negative source 344 through resistor 345 to provide a negative input to inverter 341. The positive output of inverter 341 is again inverted by inverter 347 and applied to NAND gate 316. NAND gate 316 therefore cannot be fully enabled until capacitor 346 is charged positive by the output of NAND gate 303 when the high threshold is reached. This insures a delay in the operation and release of RO relay 17, thereby holding RO relay 17 operated as L relay 16 tracks dial pulses.

Detailed Description Text (38):
It will be recalled that the sensors 33 and 34 of FIG. 1 provide linear outputs representing voltage and current, respectively, on the subscriber loop. Moreover, these voltages and currents can be of either polarity. The threshold detectors of FIG. 6 are therefore also arranged to respond to signals of either polarity and to produce outputs the significance of which is inverted when the polarity of the inputs is inverted. In order to avoid the necessity of providing separate threshold detectors for these opposite polarities, the logic of FIG. 7 is adjusted by a polarity-indicating signal on lead 125. If the line voltage is positive, for example, NAND gates 302 and 311 are enabled via resistor 327. If the line voltage is negative, NAND gates 301 and 313 are enabled via inverter 326. In this way, the NAND gates 303 and 314 respond correctly to the magnitude indication on leads 225 and 215, respectively, regardless of their polarity. For positive magnitudes, NAND gates 301 and 314 are operated through NAND gates 302 and 311, respectively, while for negative magnitudes, NAND gates 301 and 314 are operated through NAND gates 301 and 313, respectively. Since the additional logic is much cheaper and more compact than would be the additional threshold detectors, the arrangement shown in the

Figures is preferable.

Detailed Description Text (41):
The office voltage signal on lead 181 is applied to one input of NAND gate 304 and to one input of NAND gate 316 to disable relays 16 and 17 if office voltage is lost. The signal on lead 181 is also applied through inverter 334 and resistor 335 to the input of inverter 336. The input to inverter 336 is biased from positive voltage source 337 through resistor 338 and is connected to ground potential through capacitor 339. The output of inverter 336 is supplied through resistor 340 to capacitor 346. The signal on lead 181 therefore discharges capacitor 346 to reset the delay timing circuit. As previously noted, the output of inverter 341 is applied through inverter 347 to one input of NAND gate 316. The output of inverter 341 also comprises the control signal on lead 159 used to enable the output of the ringing detector of FIG. 4. The output of inverter 341 is also combined with the output of NAND gate 304 in NAND gate 348. The output of NAND gate 348 is connected so as to rapidly discharge capacitor 346, thus resetting the timing delay circuit in the operate circuit of relay 17.

Current US Original Classification (1):
379/377

Current US Cross Reference Classification (1):
379/382

Current US Cross Reference Classification (2):
379/400